

L Number	Hits	Search Text	DB	Time stamp
1	96149	map\$4 same (method or technolog\$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:06
2	15409	(map\$4 same (method or technolog\$4)) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:06
3	12099	((map\$4 same (method or technolog\$4)) and replacement) and block	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:06
4	10373	map\$4 adj3 (method or technolog\$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:06
5	1377	(map\$4 adj3 (method or technolog\$4)) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:06
6	537	((map\$4 adj3 (method or technolog\$4)) and replacement) and candidate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:06
7	467	((map\$4 adj3 (method or technolog\$4)) and replacement) and candidate) and (block or sub-network)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:06
8	464	((map\$4 adj3 (method or technolog\$4)) and replacement) and candidate) and (block or sub-network)) and select\$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:06
9	832	map\$4 adj3 technology	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:06
10	598	(map\$4 adj3 technology) and portion	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:06
21	31	(map\$4 same (method or technolog\$4)) and (divide adj block) and replace\$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:07
11	3	((map\$4 same (method or technolog\$4)) and (divide adj block)) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:07
12	118	((map\$4 same (method or technolog\$4)) and replacement) and (sub-network)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:07
13	114	((map\$4 same (method or technolog\$4)) and replacement) and block) and 716/\$.cc1s.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/09/30 08:07

14	349	(map\$4 same (method or technolog\$4)) and (replacement near5 block)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/30 08:07
15	12	(((((map\$4 adj3 (method or technolog\$4)) and replacement) and candidate) and (block or sub-network)) and select\$4) and 716/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/30 08:07
16	30	((map\$4 adj3 (method or technolog\$4)) and replacement) and 716/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/30 08:08
17	161	(((((map\$4 adj3 (method or technolog\$4)) and replacement) and candidate) and (block or sub-network)) and select\$4) and optimization	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/30 08:42
18	95	((map\$4 adj3 technology) and portion) and optimiz\$5) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/30 08:08
19	361	((map\$4 adj3 technology) and portion) and optimiz\$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/30 08:08
20	63	(map\$4 same (method or technolog\$4)) and (divide adj block)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/30 08:08
22	161	(((((map\$4 adj3 (method or technolog\$4)) and replacement) and candidate) and (block or sub-network)) and select\$4) and optimization and function\$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/30 08:43
23	25	(((((map\$4 adj3 (method or technolog\$4)) and replacement) and candidate) and (block or sub-network)) and select\$4) and optimization and function\$4) and boolean and (library or database)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/30 08:44

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040186920 A1	20040923	48	Parallel data processing architecture	710/1
2	US 20040186846 A1	20040923	48	Method of partitioning data records	707/101
3	US 20040163070 A1	20040819	49	Method and apparatus for pre-tabulating sub-networks	716/18
4	US 20040130552 A1	20040708	416	Deferred shading graphics pipeline processor having advanced features	345/506
5	US 20040125103 A1	20040701	128	Apparatus and method for volume processing and rendering	345/419
6	US 20040019857 A1	20040129	49	Method and apparatus for specifying encoded sub-networks	716/1
7	US 20040006566 A1	20040108	124	System and method for augmenting knowledge commerce	707/100
8	US 20030217350 A1	20031120	49	Method and apparatus for producing a circuit description of a design	716/18
9	US 20030217340 A1	20031120	48	Method and apparatus for performing technology mapping	716/3
10	US 20030217339 A1	20031120	48	Method and apparatus for performing technology mapping	716/3
11	US 20030217026 A1	20031120	48	Structure for storing a plurality of sub-networks	707/1
12	US 20030159116 A1	20030821	48	Method and apparatus for specifying encoded sub-networks	716/3
13	US 20030159115 A1	20030821	48	Method and apparatus for performing technology mapping	716/3
14	US 20030154449 A1	20030814	48	Method and apparatus for performing technology mapping	716/3
15	US 20030154448 A1	20030814	48	Method and apparatus for producing a circuit description of a design	716/3
16	US 20030154280 A1	20030814	48	Method and apparatus for pre-tabulating sub-networks	709/225
17	US 20030154210 A1	20030814	48	Structure for storing a plurality of sub-networks	707/102

	Document ID	Issue Date	Pages	Title	Current OR
18	US 20030131073 A1	20030710	189	Schema-based services for identity-based data access	709/219
19	US 20030093229 A1	20030515	28	System and method for improved computer drug design	702/27
20	US 20020157063 A1	20021024	1889	Implicit mapping of technology independent network to library cells	716/1
21	US 6771264 B1	20040803	104	Method and apparatus for performing tangent space lighting and bump mapping in a deferred shading graphics processor	345/426
22	US 6741983 B1	20040525	48	Method of indexed storage and retrieval of multidimensional information	707/5
23	US 6717576 B1	20040406	393	Deferred shading graphics pipeline processor having advanced features	345/419
24	US 6704873 B1	20040309	273	Secure gateway interconnection in an e-commerce based environment	713/201
25	US 5787010 A	19980728	30	Enhanced dynamic programming method for technology mapping of combinational logic circuits	716/7

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mapping <and> technology <and> function <and> layout

☐ Check to search within this result set**Results Key:****JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard**1 Global and local congestion optimization in technology mapping***Pandini, D.; Pileggi, L.T.; Strojwas, A.J.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on, Volume: 22, Issue: 4, April 2003

Pages:498 - 505

[\[Abstract\]](#) [\[PDF Full-Text \(431 KB\)\]](#) IEEE JNL
2 Combining technology mapping and placement for delay-minimization in FPGA designs*Chau-Shen Chen; Yu-Wen Tsay; TingTing Hwang; Wu, A.C.H.; Youn-Long Lin*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on, Volume: 14, Issue: 9, Sept. 1995

Pages:1076 - 1084

[\[Abstract\]](#) [\[PDF Full-Text \(792 KB\)\]](#) IEEE JNL
3 GaAs ICs for 10 Gb/s ATM switching*Nunez, A.; Sarmiento, R.; Esper-Chain, R.; Jakobsen, J.; Montiel-Nelson, J.A. Lopez, J.; Armas, V.; Tobajas, F.;*

Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1997. Technical D 1997., 19th Annual, 12-15 Oct. 1997

Pages:101 - 104

[\[Abstract\]](#) [\[PDF Full-Text \(556 KB\)\]](#) IEEE CNF
4 Delay minimal decomposition of multiplexers in technology mapping*Thakur, S.; Wong, D.F.; Krishnamoorthy, S.;*

Design Automation Conference Proceedings 1996, 33rd, 3-7 June 1996

Pages:254 - 257

[\[Abstract\]](#) [\[PDF Full-Text \(464 KB\)\]](#) [IEEE CNF](#)

5 A routability and performance driven technology mapping algorithm LUT based FPGA designs

Chi-Chou Kao; Yen-Tai Lai;

Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on , Volume: 1 , 30 May-2 June 1999

Pages:474 - 477 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(372 KB\)\]](#) [IEEE CNF](#)

6 A DSM design flow: putting floorplanning, technology-mapping, and gate-placement together

Salek, A.H.; Jinan Lou; Pedram, M.;

Design Automation Conference, 1998. Proceedings , 15-19 June 1998

Pages:128 - 133

[\[Abstract\]](#) [\[PDF Full-Text \(692 KB\)\]](#) [IEEE CNF](#)

7 Topological parameters for library free technology mapping

Reis, A.; Robert, M.; Reis, R.;

Integrated Circuit Design, 1998. Proceedings. XI Brazilian Symposium on , 30 Sept.-3 Oct. 1998

Pages:213 - 216

[\[Abstract\]](#) [\[PDF Full-Text \(36 KB\)\]](#) [IEEE CNF](#)

8 Technology decomposition using optimal alphabetic trees

Pedram, M.; Vaishnav, H.;

Design Automation, 1993, with the European Event in ASIC Design. Proceedings [4th] European Conference on , 22-25 Feb. 1993

Pages:573 - 577

[\[Abstract\]](#) [\[PDF Full-Text \(464 KB\)\]](#) [IEEE CNF](#)

9 1993 European Conference on Design Automation with the European Event in ASIC Design

Design Automation, 1993, with the European Event in ASIC Design. Proceedings [4th] European Conference on , 22-25 Feb. 1993

[\[Abstract\]](#) [\[PDF Full-Text \(20 KB\)\]](#) [IEEE CNF](#)

10 Experimental results on the impact of factorization and technology independent mapping options on multilevel synthesis

Abouzeid, P.; Besson, T.; Sakouti, K.; Saucier, G.; Gaume, F.; Roane, R.;

Euro ASIC '92, Proceedings. , 1-5 June 1992

Pages:402 - 403

[\[Abstract\]](#) [\[PDF Full-Text \(168 KB\)\]](#) [IEEE CNF](#)

11 Multilevel synthesis minimizing the routing factor

Abouzeid, P.; Sakouti, K.; Saucier, G.; Poirot, F.;

Design Automation Conference, 1990. Proceedings. 27th ACM/IEEE , 24-28 Jun 1990
 Pages:365 - 368

[\[Abstract\]](#) [\[PDF Full-Text \(324 KB\)\]](#) [IEEE CNF](#)

12 Chortle: a technology mapping program for lookup table-based field programmable gate arrays

Francis, R.J.; Rose, J.; Chung, K.;

Design Automation Conference, 1990. Proceedings. 27th ACM/IEEE , 24-28 Jun 1990

Pages:613 - 619

[\[Abstract\]](#) [\[PDF Full-Text \(488 KB\)\]](#) [IEEE CNF](#)

13 Technology mapping for standard-cell generators

Berkelaar, M.R.C.M.; Jess, J.A.G.;

Computer-Aided Design, 1988. ICCAD-88. Digest of Technical Papers., IEEE International Conference on , 7-10 Nov. 1988

Pages:470 - 473

[\[Abstract\]](#) [\[PDF Full-Text \(352 KB\)\]](#) [IEEE CNF](#)

14 Automatic synthesis and technology mapping of combinational logic

Bergamaschi, R.A.;

Computer-Aided Design, 1988. ICCAD-88. Digest of Technical Papers., IEEE International Conference on , 7-10 Nov. 1988

Pages:466 - 469

[\[Abstract\]](#) [\[PDF Full-Text \(404 KB\)\]](#) [IEEE CNF](#)

15 Prelayout estimation of individual wire lengths

Bodapati, S.; Najm, F.N.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9 , Issue: 6 , Dec. 2001

Pages:943 - 958

[\[Abstract\]](#) [\[PDF Full-Text \(351 KB\)\]](#) [IEEE JNL](#)

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